



SPEC. NUMBER

PRODUCT GROUP

Rev.P0

ISSUE DATE

PAGE
1 OF 26**Kingtech Group Co., Ltd****PV09005P0160F**

Supplier	
Model	

TITLE/SIGNATURE	DATE
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ITEM	SIGNATURE	DATE
Approved	_____	<u>2021.07.21</u>
Reviewed	_____	_____
Prepared	_____	_____



Contents

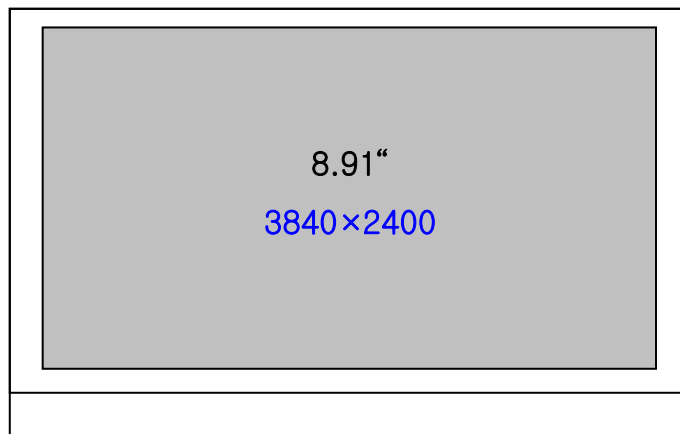
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1.0 GENERAL DESCRIPTION

1.1 Introduction

PV09005P0160F is a Black & White active matrix LTPS LCD using Low Temperature Poly-silicon TFT's (Thin Film Transistors) as an active switching devices. The LTPS-LCD has a 8.91 inch diagonally measured active area with QHD resolutions (3840 horizontal by 2400 vertical pixel arrays).



1.2 Features

- Border (L/R/U/D) : 5.0/5.0/3.0/4.0+6.0
- NTSC : Mono
- Drive IC : ST5892B



1.3 Application

1.4 General Specification

The followings are general specifications of FOG PV09005P0160F .

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	192.0(H) x 120.0(V)	mm	
CF size	202.0(H) x 127.0(V)	mm	
Number of pixels	3840(H) × 2400(V)	pixels	
Pixel pitch	50.0*50.0	um	
Contrast Ratio	≥300:1 @405nm	-	
Color gamut	Mono	-	
FOG Trans.	6.6	%	
Display mode	Normally black		
Panel Size	202.0(H) x 133.0(V)	mm	
IC	ST5892B		



2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings >

Parameter	Symbol	Min.	Max.	Unit	Remarks
LC operating Voltage [1]	VOP	-	5.0	V	Ta=25+/-2°C
Operating Temperature (Humidity)	TOP	-20	+70	°C	
Storage Temperature (Humidity)	TST	-20	+80	°C	

[1] Liquid Crystal driving voltage

Due to the characteristics of LC Material, this voltage varies with environmental temperature.



3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3. Electrical specifications >

[Ta =25±2 °C]

Parameter	Symbol	Value	Unit	Remarks
TFT Gate ON Voltage	VGH	+8	V	
TFT Gate OFF Voltage	VGL	-8	V	
TFT Common Electrode Voltage	VCOM	-0.42	V	
I/O Supply Voltage	IOVCC	3.3	V	
Liquid crystal driver supply voltage	VSP	6	V	
Liquid crystal driver supply voltage	VSN	-6	V	
Frame Frequency	f_Frame	40	Hz	

Notes :

1. VGH is TFT Gate operating voltage.
2. VGL is TFT Gate operating voltage. The low voltage level of VGL signal must be fluctuates with same phase as Vcom.
3. Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..
4. The value is just the reference value. The customer can optimize the setting value .



4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = $25 \pm 2^\circ\text{C}$) with the equipment of Luminance meter system (Goniometer system and TOPCON BM-5) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and ϕ equal to 0° . We refer to $\theta=0^\circ$ ($=\theta_3$) as the 3 o'clock direction (the "right"), $\theta=90^\circ$ ($=\theta_{12}$) as the 12 o'clock direction ("upward"), $\theta=180^\circ$ ($=\theta_9$) as the 9 o'clock direction ("left") and $\theta=270^\circ$ ($=\theta_6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or ϕ , the center of the measuring spot on the Display surface shall stay fixed.

Optimum viewing angle direction is 6 o'clock.

4.2 Optical Specifications

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	θ_3	CR > 10	70	80	-	Deg.	
		θ_9		70	80	-	Deg.	
	Vertical	θ_{12}		70	80	-	Deg.	
		θ_6		70	80	-	Deg.	
Luminance Contrast ratio		CR	$\theta = 0^\circ$	300	-	-		@405nm
FOG Transmittance		Tr		-	6.6	-	%	不帶APF&Haze @405nm
White Chromaticity		x	CIE 1931	0.298	0.308	0.318		CF @ C Light
Color Gamut (C light)				Mono			%	
Response Time (Rising + Falling)		TRT	Ta= $25 \pm 2^\circ\text{C}$ $\theta = 0^\circ$	-	-	35	ms	

**Note :**

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o' clock direction and the vertical or 6, 12 o' clock direction with respect to the optical axis which is normal to the LCD surface (see FIGURE 4).
2. Contrast measurements shall be made at viewing angle of $\Theta = 0$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see FIGURE 1) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the Value with Polarizer
4. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
5. The electro-optical response time measurements shall be made as FIGURE 3 by switching the “data” input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_r , and 90% to 10% is T_d .



5.0 Data Gate IC Pad & FPC Assignment

5.1 IC Pin Assignment



5-2. FPC Pin Assignment

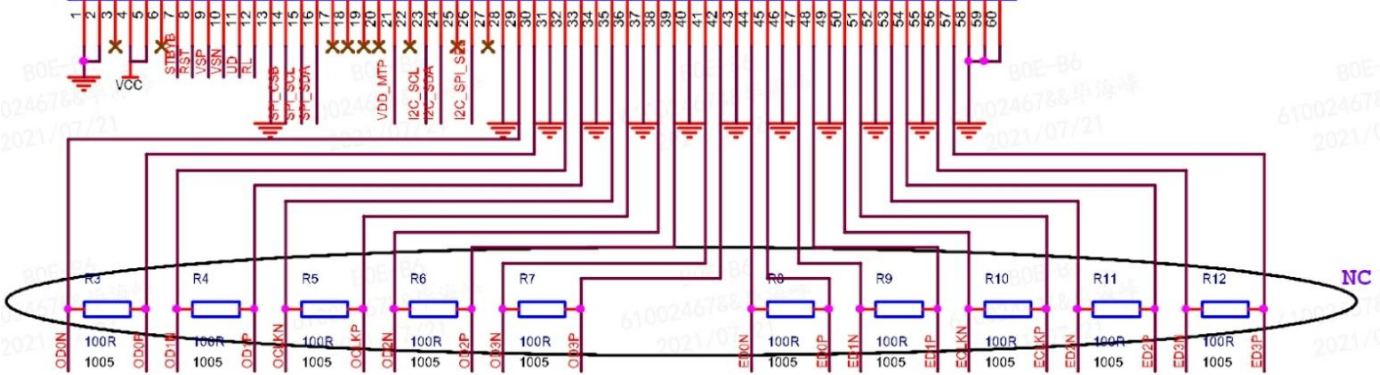
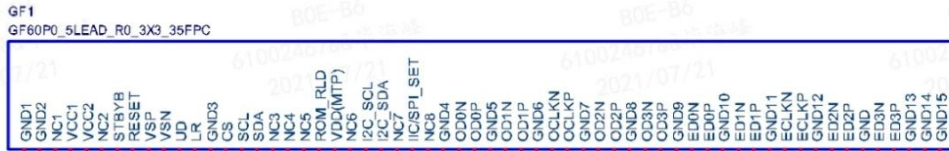
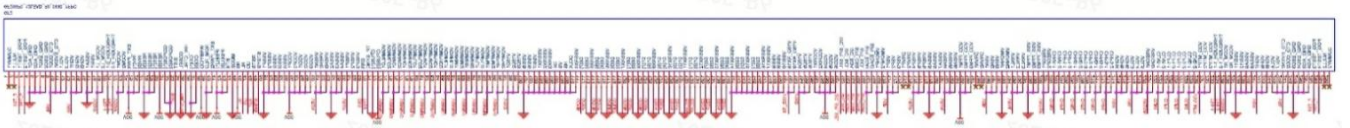


5-4. FPC Pin Map

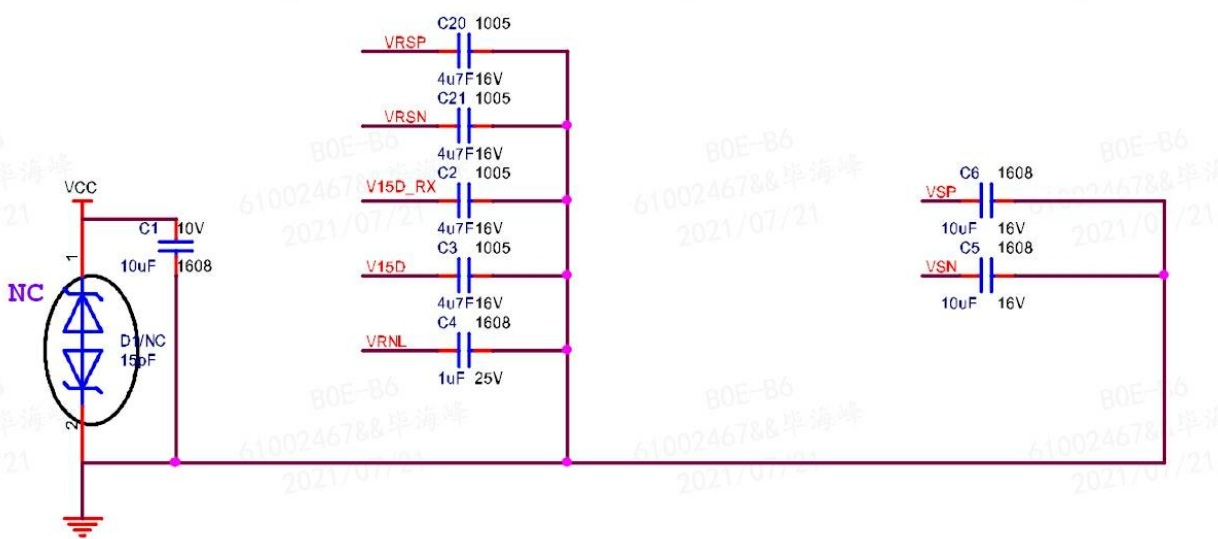
Pin No.	Pin Name	Pin Description	Pin No.	Pin Name	Pin Description
1	GND	ground	31	GND	ground
2	GND	ground	32	OD1N	- LVDS differential data 1 (ODD)
3	NC	Not connect	33	OD1P	+ LVDS differential data 1 (ODD)
4	VCC	Power +3.3V	34	GND	ground
5	VCC	Power +3.3V	35	OCLKN	- LVDS differential clock (ODD)
6	NC	Not connect	36	OCLKP	+ LVDS differential clock (ODD)
7	STBYB	Standby mode	37	GND	ground
8	RESET	Reset Pin. Low active	38	OD2N	- LVDS differential data 2 (ODD)
9	VSP	VSP	39	OD2P	+ LVDS differential data 2 (ODD)
10	VSN	VSN	40	GND	ground
11	UD	Gate output shift vertical direction select	41	OD3N	- LVDS differential data 3(ODD)
12	LR	Source output shift horizontal direction select	42	OD3P	+ LVDS differential data 3 (ODD)
13	GND	ground	43	GND	ground
14	CS	Chip select signal for SPI interface	44	ED0N	- LVDS differential data 0 (EVEN)
15	SCL	Clock signal for SPI interface	45	ED0P	+ LVDS differential data 0 (EVEN)
16	SDA	Serial address and data input/output for spi	46	GND	ground
17	NC	Not connect	47	ED1N	- LVDS differential data 1 (EVEN)
18	NC	Not connect	48	ED1P	+ LVDS differential data 1 (EVEN)
19	NC	Not connect	49	GND	ground
20	ROM_RLD	MTP reload per 30 frames(NO CONNECT)	50	ECLKN	- LVDS differential clock (EVEN)
21	VDD(MTP)	Power supply for MTP circuit	51	ECLKP	+ LVDS differential clock (EVEN)
22	NC	Not connect	52	GND	ground
23	I2C_SCL	Not connect	53	ED2N	- LVDS differential data 2 (EVEN)
24	I2C_SDA	ground	54	ED2P	+ LVDS differential data 2 (EVEN)
25	NC	Not connect	55	GND	ground
26	IIC/SPI_SELECT	Serial interface selection	56	ED3N	- LVDS differential data 3 (EVEN)
27	NC	Not connect	57	ED3P	+ LVDS differential data 3 (EVEN)
28	GND	ground	58	GND	ground
29	OD0N	- LVDS differential data 0 (ODD)	59	GND	ground
30	OD0P	+ LVDS differential data 0 (ODD)	60	GND	ground



5-5.Schematic Design



POWER FILTERING

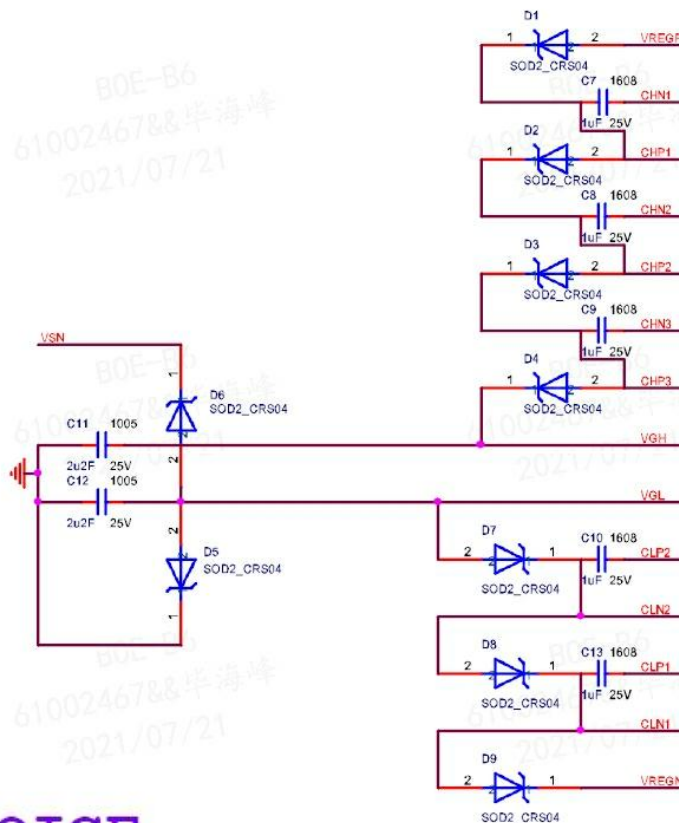




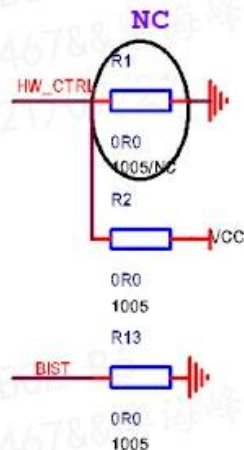
5-5.Schematic Design

CHARGE PUMP

- VGL VGL
- VGH VGH
- VCOM VCOM
- TR2 TR2-1
- TR2 TR2-2
- TR1 TR1-1
- TR1 TR1-2
- F_TS F_TS1
- F_TS F_TS2
- F_TS F_TS3
- F_TS F_TS4
- ERR ERR
- TPSY TPSY



HW CHOICE



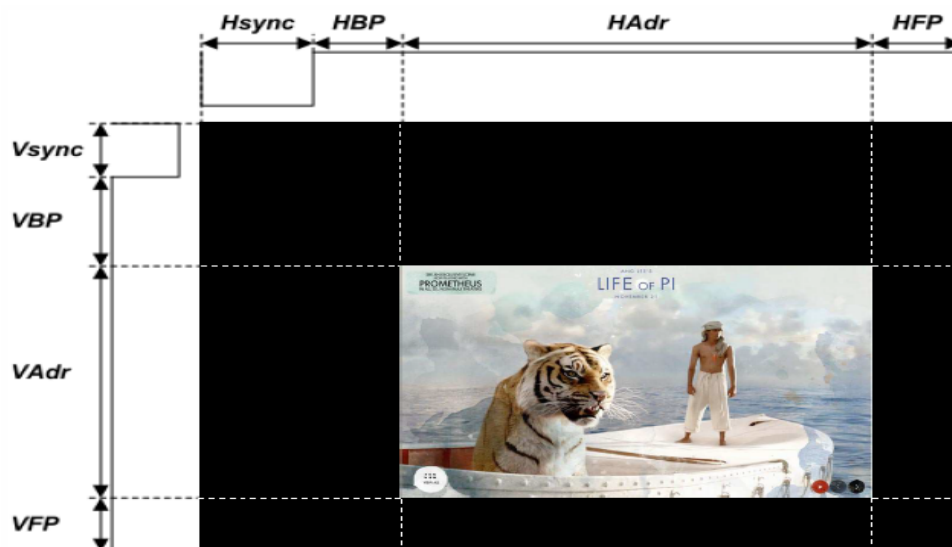


3.6 Interface timing Parameter

< Table12. Timing Parameter >

Item		Symbol	min	typ	max	UNIT	
LCD	Frame Rate	-	-	40	-	Hz	
Timing	DCLK	Frequency	fCLK	67	72	84	MHz
	Horizontal	Horizontal total time	tHP	692	730	830	tCLK
		Horizontal Active time	tHadr	640			tCLK
		Horizontal Pulse Width	tHsync	2	20	30	tCLK
		Horizontal Back Porch	tHBP	20	30	80	tCLK
		Horizontal Front Porch	tHFP	30	40	80	tCLK
	Vertical	Vertical total time	tvp	2422	2450	2520	tH
		Vertical Active time	tVadr	2400			tH
		Vertical Pulse Width	tVsync	2	10	20	tH
		Vertical Back Porch	tVBP	10	20	50	tH
Vertical Front Porch		tVFP	10	20	50	tH	

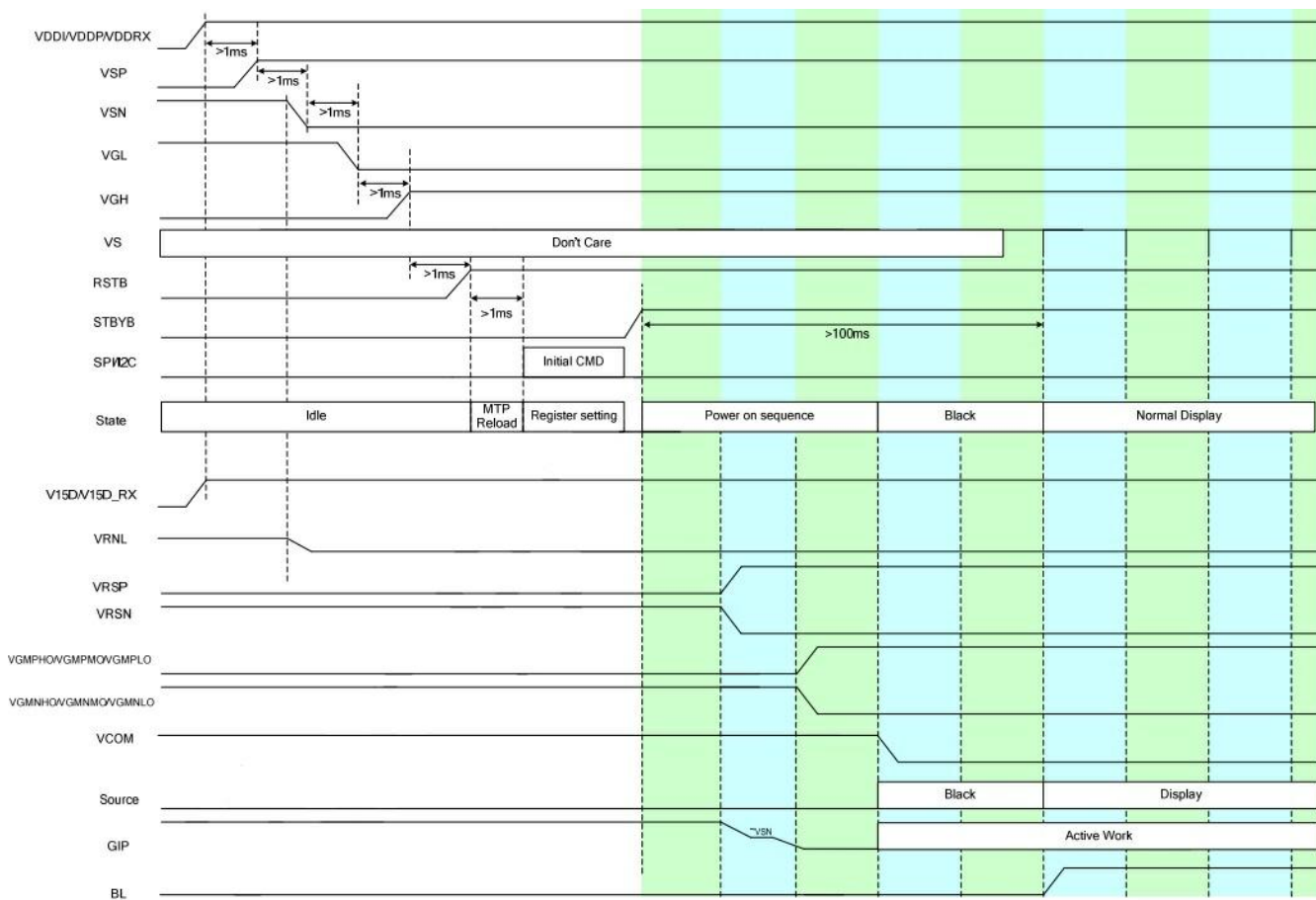
- Remarks : 1.This production is 2port
- 2.The production transmission diagram is 1280RGBx2400





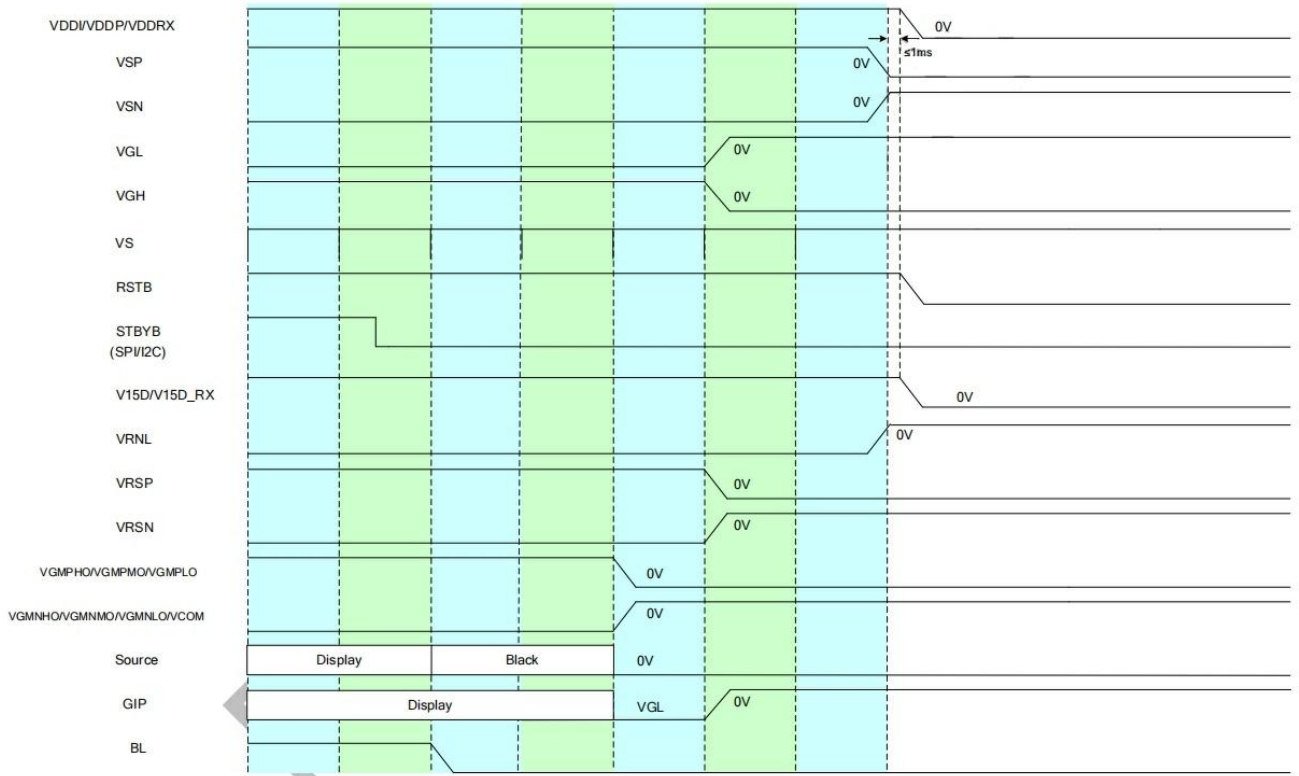
3.8 Power Sequence

Power on





Power off





7.0 APPENDIX

Figure 1. Optical Test Equipment Setup

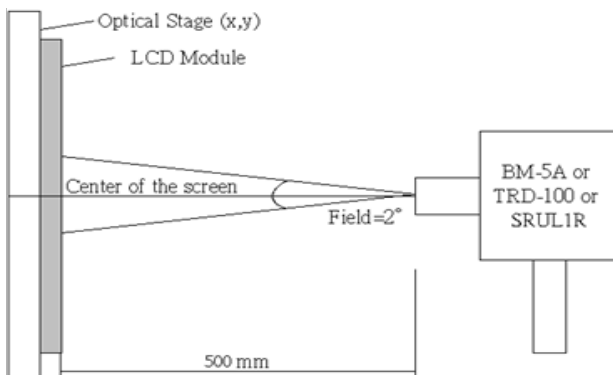


Figure 2. Response Time Testing

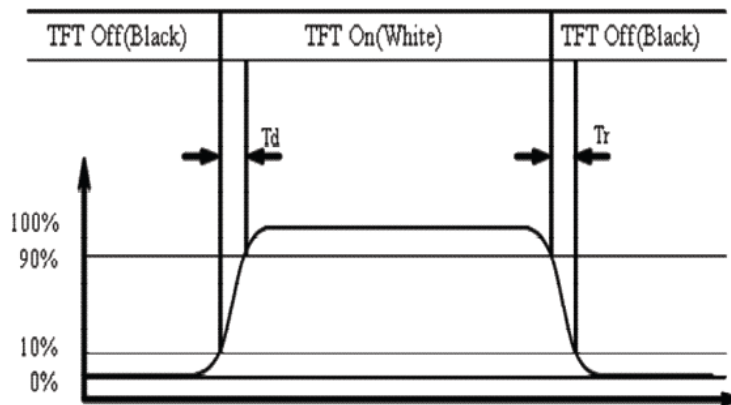


Figure 3. The Definition of V_{th} & V_{sat}

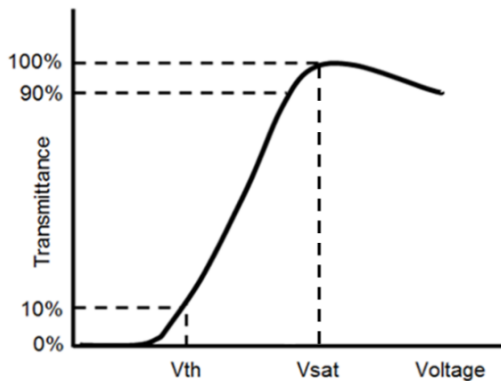




Figure 4. Viewing Angle Range is defined as follows;

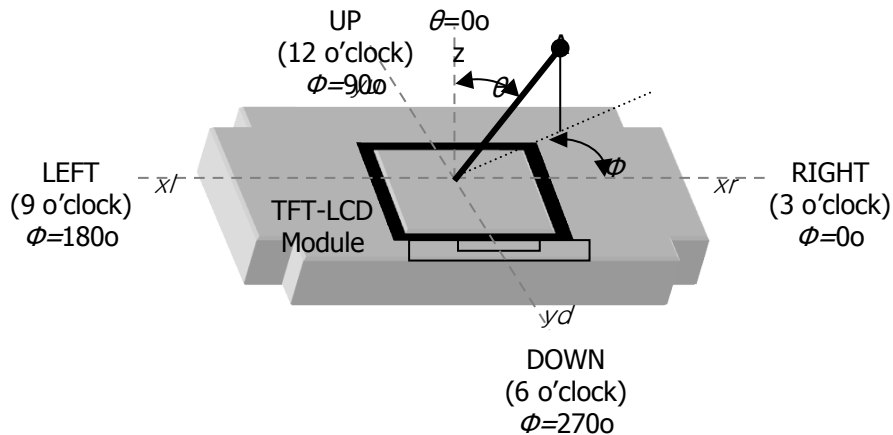
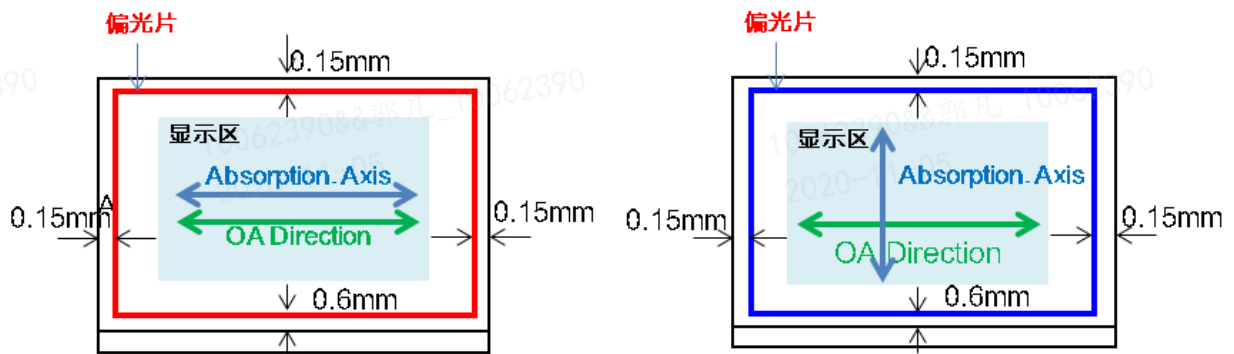


Figure 5. Pol General Spec

UP POL

DOWN POL



	CF Pol	TFT Pol	Remark
Absorption. Axis	0°±0.5°	90°±0.5°	住化\日东



8.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

<Table 8. Reliability test>

No	Test Items	Conditions
1	High temperature storage test	Ta = 80 °C, 240 hrs
2	Low temperature storage test	Ta = -20 °C, 240hrs
3	High temperature & high humidity operation test	Ta = 60 °C, 90%RH, 240hrs
4	High temperature operation test	Ta = 70 °C, 240 hrs
5	Low temperature operation test	Ta = -20 °C, 240hrs
6	Thermal shock test	Ta = -20 °C ↔ 80 °C (30min), 100cycle